Claims

What is claimed is:

[c1] A bump and vias structure, comprising:

a metal layer;

a plurality of vias connecting the metal layer to another metal layer;

a bump mounted on the metal layer; and

a first slot formed in the metal layer between the vias and the bump.

[c2] The bump and vias structure of claim 1, wherein the bump is mounted on the metal layer via a landing pad.

[c3] The bump and vias structure of claim 1, further comprising second and third slots disposed between the first slot and the bump.

[c4] The bump and vias structure of claim 3, wherein the second and third slots are displaced laterally along the metal layer and form an aperture therebetween that is centered with respect to the first slot.

[c5] The bump and vias structure of claim 1, wherein the first slot comprises a section of the metal layer that is evacuated of conductive material.

[c6] The bump and vias structure of claim 1, wherein the first slot comprises a current-resistant material.

[c7] The bump and vias structure of claim 1, wherein the first slot comprises a dielectric material.

[c8] An integrated circuit, comprising:

a metal layer;

a plurality of vias connecting the metal layer to another metal layer;

a bump mounted on the metal layer; and

a first slot formed in the metal layer between the vias and the bump.

[c9] The integrated circuit of claim 8, wherein the bump is mounted on the metal layer via a landing pad.

[c10] The integrated circuit of claim 8, further comprising second and third slots disposed between the first slot and the bump.

[c11] The integrated circuit of claim 10, wherein the second and third slots are displaced laterally along the metal layer and form an aperture therebetween that is centered with respect to the first slot.

[c12] The integrated circuit of claim 8, wherein the first slot comprises a section of the metal layer that is evacuated of conductive material.

[c13] The integrated circuit of claim 8, wherein the first slot comprises a current-resistant material.

[c14] The integrated circuit of claim 8, wherein the first slot comprises a dielectric material.

[c15] A method for reducing current crowding in a bump and vias structure, comprising:

determining a length of a first current path between a first via and a bump;

determining a length of a second current path between a second vias and the bump; and

disposing a slot along one of the first and second current paths depending on the first and second current path lengths.

[c16] The method of claim 15, wherein disposing the slot is dependent on whether the first current path length is longer than the second current path length.

[c17] The method of claim 16, wherein if the first current path length is longer than the second current path length, the slot is disposed along the second current path.

[c18] The method of claim 15, further comprising disposing at least one additional slot between the first slot and the bump.